

# PLASTIC DIGITAL ARRAY BEAMFORMER DEVELOPMENT WITH INTEGRATED HIGH EFFICIENCY GALLIUM-NITRIDE MMICs

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## ABSTRACT

With the advent of highly efficient wide bandgap amplifiers, there is the possibility of generating high power outputs without using expensive packaging. The goal is to create a plastic panel of integrated radiators which have limited cooling while having an output with a minimum of 25 Watts per element with efficiencies above 60% at die level. Towards this end, the development of highly efficient GaN MMICs and plastic packaging is being investigated. To create the MMIC amenable for integration with a patch antenna on the backside of the PCB material, the packaging challenge is to have the high power signal flow down through the board while the heat flows in the opposite direction, up through a heat sink. In this paper, we report the performance of plastic packaged amplifiers and discuss their integration into a 16-element digital array radar

## INTRODUCTION

Conventional phased array radars dissipate heat on the order of hundreds to thousands of kilowatts (Wilson, 2001). Many radar systems typically will have a single RF generator and a series of phase shifters, which provide the beam steering. Due to the strong temperature dependencies of the phase shifters these systems require advanced cooling systems to allow the radar system to operate as intended. In addition to the required thermal management, these systems are relatively inflexible with regard to software-defined beam forming.

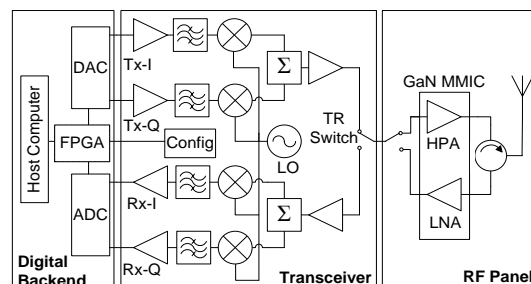
Active arrays are increasingly popular, but can be expensive to realize in practice. With the advent of highly efficient wide bandgap amplifiers, there is now the possibility of generating high power outputs while using relatively inexpensive packaging in a modern active array architecture with element-level amplitude/phase control and power generation. Furthermore, implementing a digital backend on the radar enables dynamic beamforming and flexible analysis of the received data; this opens the door for multiple receive beams and multiple target tracking, waveform diversity applications such as MIMO radar (Fishler, 2004), and computerized adaptive jammer suppression (Wirth, 2001). The separation and digitization of each Tx/Rx chain allows the SNR and phase noise requirements to be lowered by  $10\log N$  dB in the active phased array for uncorrelated additive and phase noise, allowing COTS communications electronics components to be used at the

element level. There is no need for a phase shifter or time delay element in each transmit/receive (T/R) module. This allows for a simplified transceiver architecture with reduced component complexity and higher performance. This architecture is highly amenable to a two chip solution, a high power front end, made of widebandgap materials such as GaN, and a highly integrated backend, such as SiGe or CMOS.

The goal of the Digital Array Radar (DAR) Project managed by the U.S. Army Communication-Electronics RD&E Center (CERDEC) is to develop a digitally controlled radar system, implementing highly efficient wide bandgap amplifiers into a subpanel form factor. To this end, Purdue is designing and developing a 16-element array for a phase-array radar proof of concept demonstration from the ground up, starting with package-level integration of GaN amplifiers, to the development of the RF panel, and finally system-level control using a full digital backend. In this paper, we focus on the capability of integrating the high power MMIC's into a low cost plastic radiating panel.

## 1. SYSTEM OVERVIEW

The concept for this project is to design an adaptable radar system that is capable of digital beamforming with high power output per element integrated into a planar panel. The radar has a digital backend that is actively controlling the phase and amplitude of each individual element. Signal generation is done through FPGAs to generate the required in-phase and quadrature signals at baseband through 12-bit, 24 MSPS DACs. The baseband signal is then directly up-converted to RF through a 2x2 MIMO SiGe WiMAX direct-conversion transceiver from Sierra Monolithics.



**Figure 1.** Schematic of a single channel, where one FPGA and Host Computer control multiple channels.

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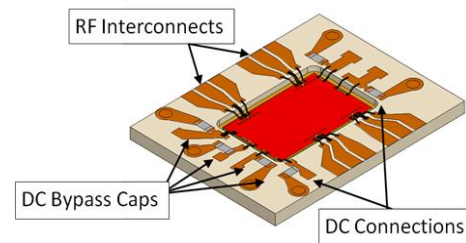
The signal is then amplified by a Cree GaN HPA on the RF panel and transmitted through a patch antenna integrated into the host panel. The received signal is amplified by a GaN LNA to enhance linearity, then is down-converted to baseband using the transceiver, and input to the FPGAs following digitization using 12-bit, 24 MSPS ADCs. The schematic of one element in the array is shown in Figure 1.

The desired high output power per radiating element is achievable through highly efficient GaN MMIC with PAE approaching 65%. Because of the high efficiency, the advanced thermal management systems used in many of the current phased-array radar systems is no longer necessary. Where cooling plates or liquid cooling methods were once required to maintain correct operation, little or no air flow may provide the desired performance. In addition, less expensive materials can now be used to design the package and RF panel. Instead of using more expensive materials, the packages are made out of plastic. Along with the use of plastic packaging, which is enabled by the low dissipated power from the high efficiency amplifiers, the antenna panel is also made with lightweight, low-cost plastic substrates. This allows the use of standard manufacturing processes to build multilayer organic boards. The panel is populated using primarily COTS components, many of which are becoming inexpensively available with the advent of the rising WiMAX market.

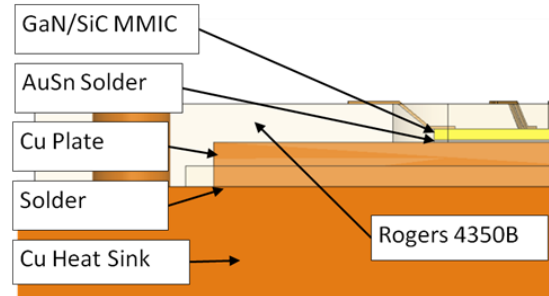
## 2. PACKAGE LEVEL INTEGRATION

The first effort towards the development of the 16-element digital, phased-array radar proof-of-concept was the development of the package to house the Cree GaN MMIC. The package was designed using Rogers 4350B, a plastic material with consistent electrical properties at the desired temperature range, from ambient to over 150°C. The package is illustrated in Figure 2. The package is made of a single layer of plastic substrate on a copper pad, and has RF interconnects and DC connections. The GaN MMIC contains an HPA and LNA on the same chip, with the biasing and RF interconnects of the two amps being completely independent from one another. The package was designed to sink the self-heating from the amplifier downwards, while keeping the RF and DC biasing connections on the upper side. This is different from traditional QFN packages, where the heatsink and package leads are on the same side. In keeping the thermal path separated from the RF path, it prevents the heatsink from interfering with the antenna's functionality, which is integrated in the layers below the GaN amplifier package. If it were a traditional QFN package, the heat would have to be dissipated through the antenna side, with the heatsink effecting the RF performance.

The thermal path for this package is shown in Figure 3. It consists of the amplifier die, which is soldered, with approximately a 1mil layer of gold tin solder, to a 15mil copper die pad that is in turn soldered, using lead tin solder, to a heat sink. The copper die pad serves as a heat spreader and as the bottom of the package. The size and density of the materials effects how quickly it can change in temperature. Typical thermal time scales are on the order of microseconds for the MMIC, seconds for the package, and minutes for the system (Wilson, 2001). These time scales are important to consider because the temperature of the junctions will increase during the transmit pulse. This increase in temperature has the potential of changing the device performance, including power droop and phase changes. This also implies that the junction temperature will be significantly hotter than the base plate during operation, and consequently in terms of reliability the device will be subjected to harsher thermal conditions.



**Figure 2.** Package Design



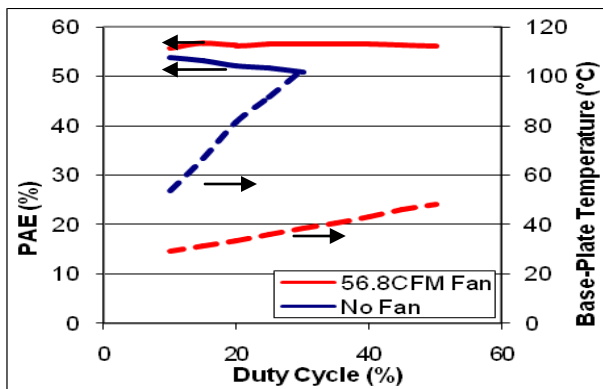
**Figure 3.** The thermal path of the package

One of the major benefits of using wide bandgap transistors for amplifiers is their ability to generate high powers with high efficiency. In this study, the desired minimum of 25W of output power is achievable with the amplifier approaching 65% PAE for on chip measurements. This implies that at least 14W total is dissipated from the HPA while it is turned on. For the radar applications, the expected duty cycle is relatively low, generally 10%, which significantly decreases the time-averaged dissipated thermal power. As the duty cycle increases, the effective dissipated power also increases. This dissipated power directly corresponds to the junction temperature of the amplifier. As the junction temperature increases, the performance of the amplifier decreases, because the gain and drain current of the amplifier decrease as the device transconductance

decreases with the increase of temperature (Nuttinck, 2001). This is important because it is what fundamentally defines the need for a thermal management system. Characterizing this decline in performance is necessary to find the required cooling system for the panel.

## 2.1 Amplifier Performance at Varying Duty Cycles

The thermal management system which is required to maintain acceptable amplifier performance is critical to successfully making a panelized high power radiator. The two simplest evaluated approaches involve using a standard PC board heat sink both with and without a typical PCB fan. For the evaluation, a connectorized version of a packaged HPA was operated which otherwise had the same components as the panel. The duty cycle of the device was varied between 10% up to 50% to increase the average self-heating power dissipation in the amplifier. Testing was conducted at 3.3GHz with a 1kHz period. The amplifier had a peak PAE of nearly 57% in the package operating with a heat-sink temperature of 32°C at 15% duty cycle when tested with a typical PCB fan (56.8CFM), as shown in Figure 4. There is around 0.3dB of loss in the line between the die and output SMA interconnect in the connectorized package. This amount of loss results in approximately a 4% decrease in PAE for the connectorized tests. At the die level, the amplifier is near 65% efficient, implying that the device is operating almost as ideally expected at 15% duty cycle. At the same operating conditions with no fan applied, the PAE was still 53% with a heat sink temperature of 67°C. When tested up to 30% duty cycle with no fan, it maintained a PAE of 50.8% and heat-sink temperature of 103°C, a decrease of only 6.2% compared to peak performance.



**Figure 4.** The GaN HPA PAE and Base-Plate Temperature as a function of Duty Cycle.

The uncooled performance is not dramatically worse, showing that the amplifier can be used even without a cooling fan, at least at room temperature conditions. Modern phased-array radar systems can require liquid cooling and other advanced cooling methods to maintain the needed device performance

(Price, 2003). The tests show that it may be in the realm of possibility to have a full radar system that uses only localized cooling, such as small fans, or even with no fans at all when operating at room temperature, instead of large cooling manifolds.

## 2.2 Predicting Amplifier Parameters and Temperature with a Drain Current

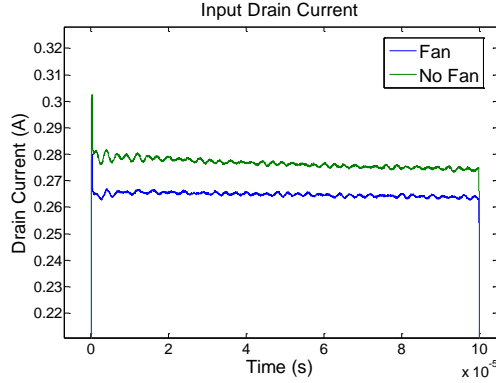
Amplifier performance predictably changes as a function of junction temperature, making it possible to characterize a temperature sensitive electrical parameter, or TSEP, to be able to use it as a thermometer (EIA/JEDEC, 1995). In the case of GaN, the drain current has been used for this purpose. In one such approach, short pulses were used to obtain the drain current, without significant self-heating (Conway, 2008). The EIA/JESD51-1 Standard from JEDEC also outlines a procedure for the collection of this data and how to use it to determine the temperature (EIA/JEDEC, 1995). Following a similar method to the standard, the data for this test was collected using a thermal chamber to provide the temperature control. Short pulses with a small duty cycle were used to minimize the effect of self-heating. The pulse itself was 2us long, with a 100ms period. According to a transient thermal simulation of short, dissipated power pulses, the self-heating effects during this test should have caused less than a few degrees Celsius rise in temperature and allowed enough time for the junctions to cool to the chamber temperature. The transient drain current for both amplifier stages was monitored, as well as the time domain output RF power pulse. The temperature sweep was from around 30°C to 90°C with 5°C increments.

Testing has shown that the input stage and output stage both have a drain current that linearly declines as a function of temperature. The output RF power, corresponding to a decline in the gain, also decreases. Applying a linear curve fit to the two current data sets for both amplifier stages provides a means to determine the average junction temperature. The output power and PAE can also be used to determine the approximate die temperature, but it is not as desirable as knowing individual junction temperatures.

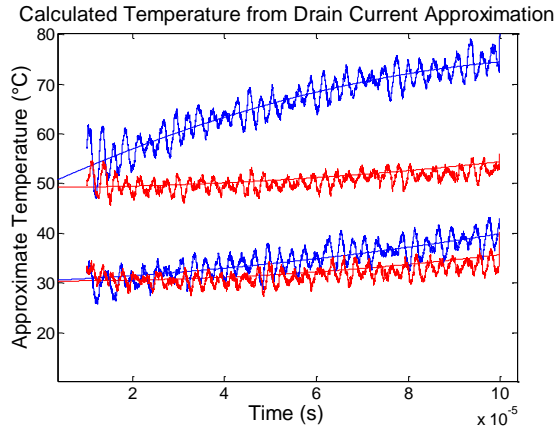
## 2.3 Self Heating Effects on Operational Pulses

The amplifier was then subjected to a 100us pulse with a 1ms period, sufficient for creating self-heating. Data sets were collected after the amplifier reached thermal stability, both with and without a fan. The drain current is lower when the amplifier was operated without a fan, and is consequently at a higher temperature, as expected given the slope for the input stage. The input drain current is shown in Figure 5, where it can be seen that there is a slight decrease as a function of time due to

self heating. With the slope from the characterized drain currents as a function of temperature, the data from Figure 5 can be used to calculate transient junction temperature. The current does have a slight initial spike, due to the DC switch, which is likely the reason for the small oscillations seen across the pulse. Despite this, it is clear that the current decreases over time as a result of self heating.



**Figure 5.** The input stage drain current, with and without a fan



**Figure 6.** Approximate junction temperature of input (red) and output (blue) stages with (below) and without (above) a fan

Knowing the base-plate temperature and the initial performance at the beginning of the pulse, the y-intercept was calculated. This was used in conjunction with the slope to determine the estimated transient change in temperature. The results of this calculation are shown in Figure 6 for 10% duty cycle with and without a fan cooling the package. It can be seen that the small variations due to slight instability in the current signal effects the instantaneous temperature swing. Because of this, this method is primarily a helpful to estimate the junction temperature within a 5 degree range, rather than an exact value. The value is in determining approximately how much hotter the junctions are over the heat sink temperature. The input stage has the highest dissipated power density and as a result reaches upwards

of 80°C when no fan is used, according to this data. As shown in Figure 6, the junction temperatures of the HPA are up to 30°C lower with the fan implemented. While operation without a fan may yield acceptable RF performance, the additional rise in temperature could have an impact on device reliability.

To validate the calculated junction temperatures, transient thermal simulations were done using Ansoft's ePhysics. These simulations modeled the pulsed thermal power dissipated on the HPA at a specified initial temperature. The results of the simulation are given in Table 1 along with the calculated data for both stages of the amplifier. The data is for three duty cycles using a fan for cooling. As it can be seen in Table 1, using the drain current to determine the temperature provides a reasonable means for getting an approximate value, with the errors most likely being from difficulties in modeling the heat sink path due to material non-idealities. Overall, the clear lesson is that the efficiency in the amplifier leads to suitable performance in the plastic panel arrangement.

Duty Cycle	Input Stage Calculated	Input Stage Simulated	Output Stage Calculated	Output Stage Simulated
10%	39.87°C	38.33°C	35.67°C	36.29°C
20%	44.46°C	40.57°C	38.04°C	38.42°C
30%	44.75°C	41.63°C	38.92°C	37.97°C

**Table 1.** Calculated and simulated junction temperatures

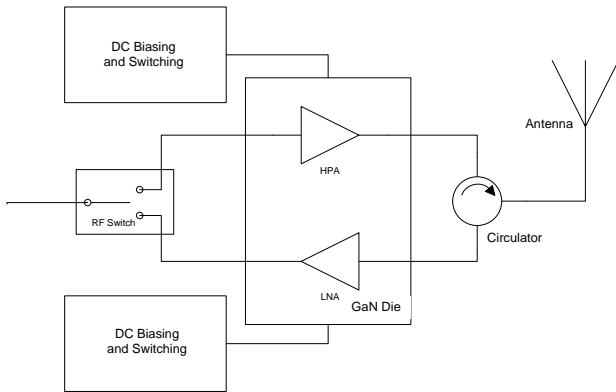
## 2.4 Performance in a Test Panel

The T/R GaN chip, which incorporates an LNA and HPA on a single die, was packaged and built into an example 2x1 array panel, which integrates the required dc switching and patch antenna into the host board. With only using a 18x6.3x13.4mm copper block as a heat sink, one of the HPA's was able to output large amounts of RF power with minimal cooling systems. At a typical drain bias of 28V, the panel radiated 28W from the one element with an overall efficiency of around 41% (including the circulator and antenna losses), while maintaining a heat sink temperature of 52.5°C. Operating the amplifier at similar operating conditions only with no fan, the element of the panel radiated 20W with a base plate temperature of 74.4°C. This shows that the panel is still capable of operating at high temperatures, without a significant loss of performance. The antenna panel has approximately 0.1dB of line loss, 0.5dB of circulator insertion loss, and 0.5dB of loss due to the antenna. This results in 1.1dB of loss between the HPA output and the antenna output. This correlates to a decrease in PAE of around 12% from the die-level and an overall amplifier PAE of 53%. This shows that while good thermal management can slightly improve performance, as seen in Figure 4, the thermal effects are marginal relative to the other system losses. Increased performance enhancements should not focus on the thermal rather the antenna, transmission line, and antenna losses.



### 3. PANEL LEVEL INTEGRATION

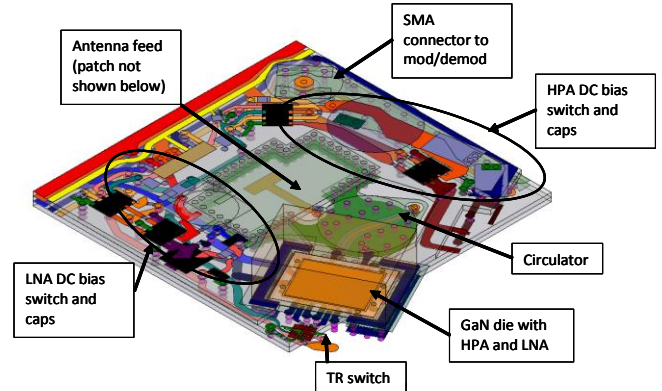
The use of individual GaN amplifiers for each element of a phased array, along with a single chip IQ modulator, makes it feasible to consider integrating a panelized radar system on a single panel. Already the integration of the entire RF transmit-receive chain into a plastic panel (made of Rogers 4350, a material very similar to FR4) has been demonstrated at Purdue. This allows for an extremely flexible and yet inexpensive digital phased array.



**Figure 7.** Block schematic of single element of RF board

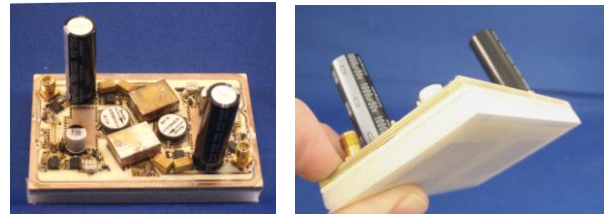
The simplified topography of the transmit-receive chain is shown in Figure 7. On transmit, the signal coming from the IQ modulator travels through the T/R switch, into the GaN HPA, through the circulator and out the antenna.

Building such a panel is not without its challenges, such as dissipating the heat from high power GaN elements. However, as has been already discussed, this is achievable due to the high efficiency of the GaN HPA. To be able to switch the HPA on and off quickly, a large amount of instantaneous DC power (between 1.2 and 2 amps at 28 volts) is required, making it necessary to have a large amount of charge storage near the HPA. This takes the form of a 1000  $\mu\text{F}$  low ESR capacitor in parallel with several smaller capacitors. If these capacitors are not big enough, or have too much ESR, or are too far from the GaN, the HPA will be prone to severe oscillations.

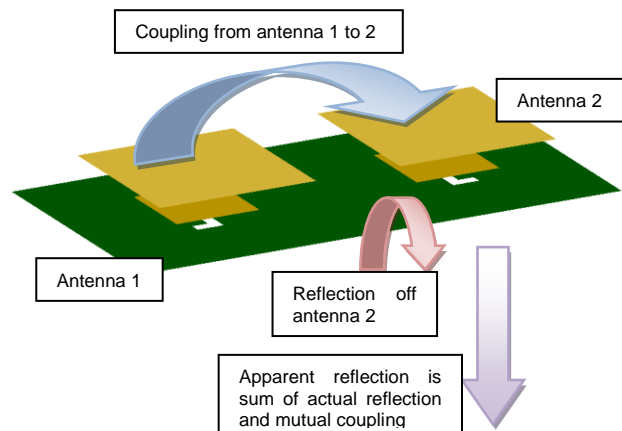


**Figure 8.** Layout of one RF panel element

All of this must be accomplished in the smallest amount of space possible, so as to keep the circuitry per element in an element sized space (allowing panels to be tiled next to one another). The layout of a single element is shown in Figure 8. Note that the HPA bias switch and the SMA connector pads pictured there are actually associated with the adjacent element to the lower right of the element pictured. Similarly, the HPA bias switch and SMA connector for the pictured element are actually located in the adjacent element's area to the lower right. This was done to conserve space and keep bias capacitors as close as possible to the HPA itself. What this effectively means is that we have blocks of two elements which are completely self-contained and repeatable in an n-dimensional array.



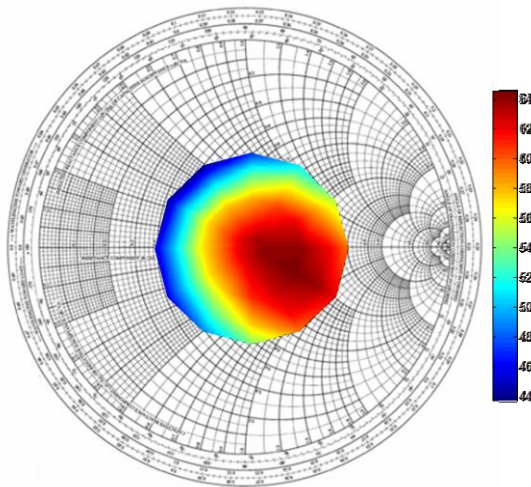
**Figure 9.** Completed 2 element RF board



**Figure 10.** Mutual coupling and reflection of antennas

### 3.1 Mutual Coupling

In order to be able to eventually integrate the entire radar system onto a single panel, the antenna used is a slot coupled stacked patch antenna. In the absence of any other antennas in the near field, it is possible (and has been discussed in many books and papers) to design a patch antenna that has very low reflection over a reasonable bandwidth. However, the mutual coupling from nearby antennas makes this much more difficult, as the apparent reflection from an antenna is comprised of the actual mismatch of the antenna and the power from mutual coupling of nearby antennas (Figure 10). The mutual coupling can add in phase or out of phase with the reflection; making an apparent change in input impedance as a function of scan angle. Our antennas are optimized for minimum reflection at broadside. When the scan angle changes, the amplitude and phase of the signals change, which means the effective impedance of the array does as well. This is important in the DAR because the GaN HPAs require a low reflection coefficient to maintain their high-efficiency, high power operating point. As an example, the simulated efficiency as a function of reflection coefficient at 3.2 GHz for the GaN HPA is shown below. Efficiency can drop nearly 20 points at a reflection coefficient just over 10 dB. Therefore, controlling the mutual coupling is essential to proper panel performance even with well matched antennas.



**Figure 11.** Efficiency of HPA as a function of output impedance

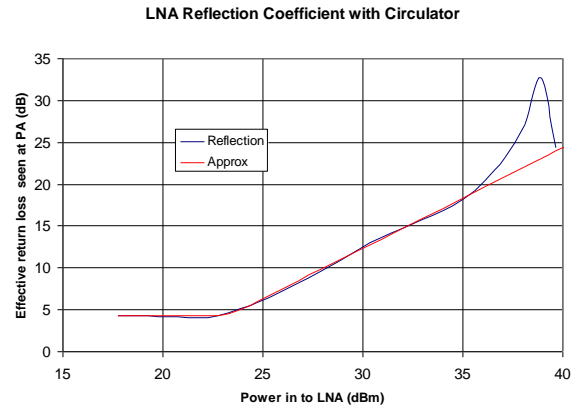
### 3.2 Mitigation of Mutual Coupling

The use of a circulator provides some measure of protection from this effect, but it is limited by the extent to which the LNA can absorb the coupled RF energy. Fortunately, the GaN LNA can absorb a substantial amount of power without changing its performance

characteristics afterwards. This is yet another advantage of using such a robust technology.

When the LNA is turned off (in pinch-off with zero drain voltage), the reflection coefficient off of the input to the LNA is not particularly low – on the order of only 3 or 4 dB. It turns out that, given sufficient input power, the gate of the LNA will begin to conduct, allowing the RF energy to be absorbed. A commercial WiMAX circulator with an isolation of about 20 dB was used to measure this power-dependent effective reflection coefficient, and the non-linear results are shown in Figure 12.

Note that the measured effective return loss increases linearly with input power after about 23 dBm with a slope of 12 dB/decade, up to the limit of the circulator's isolation spec. as shown in the approximation in the figure. This indicates that when the GaN HPA is operating in its high power regime (> 25 Watts or 44 dBm), if the sum of all of the effective mutual couplings from adjacent antenna/PA combinations is higher than about 23 dBm, the LNA begins to effectively absorb the power, thus protecting the HPA by shielding it from load-pulling effects and allowing it to maintain its high efficiency.



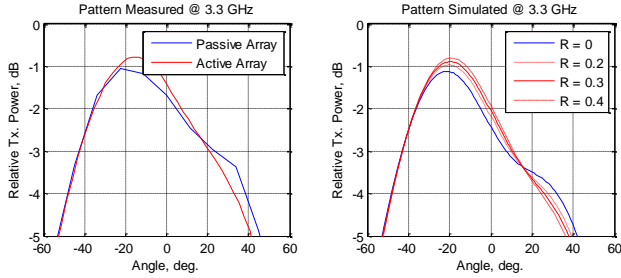
**Figure 12.** LNA reflection coefficient as a function of Input Power as seen through a WiMAX circulator

### 3.3 Validation of Circulator/LNA Properties

As an example of this, the 2x1 GaN panel that was tested has a mutual coupling between antenna elements of around 15.4 dB. For a transmit power of 22 Watts (43.4 dBm) output one would expect, based on Figure 10, an effective reflection coefficient of right around 10 dB. While it is impossible to actually measure this on the fully-integrated panel, an approximate value of the effective reflection coefficient can be determined by looking at the degradation in the antenna pattern caused by re-reflections off of the amplifiers. The measured antenna pattern of the 2x1 array is given to first-order approximation by:

$$F_{\text{meas}}(\theta) = F(\theta) + \Gamma S_{21} F(-\theta) \quad (1)$$

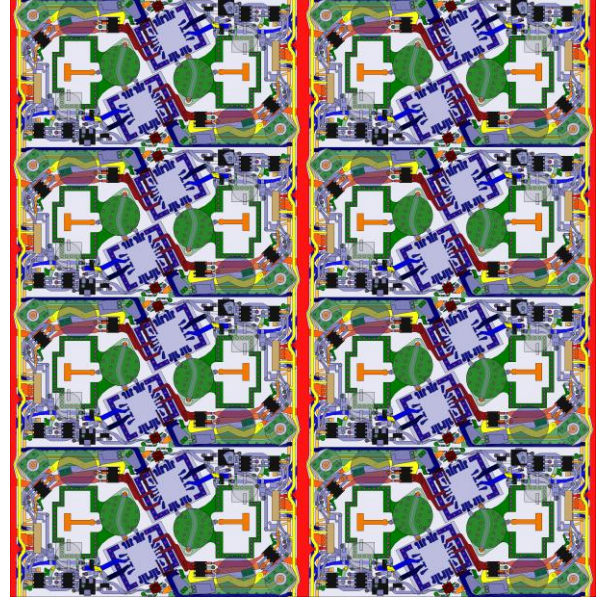
where  $F(\theta)$  is the individual element pattern of the transmit antenna,  $F(-\theta)$  is, by symmetry, the pattern of the coupled antenna,  $S_{21}$  is the mutual coupling, and  $\Gamma$  is the effective reflection coefficient off of the RF frontend of the coupled element. The measured difference between the terminated ( $\Gamma = 0$ , in blue) and active ( $\Gamma$  determined by RF frontend and power level, in red) antenna patterns are shown in the left column of Figure 12 for the aforementioned transmit power of around 22 Watts at 3.3GHz. On the right side of the figure are plots of the simulated pattern for  $\Gamma = 0$  (blue) and  $|\Gamma| = 0.2$ ,  $|\Gamma| = 0.3$ , and  $\Gamma = 0.4$  with a reflection angle of 100 degrees; this angle is chosen because it gives the correct overall “shape” in the deviation from the nominal pattern. The measured deviation is very close to what was simulated with an effective  $|\Gamma|$  between 0.3 and 0.4, indicating that a reflection coefficient in the range of 10dB (0.316) is entirely reasonable. This validates the idea that, in the high power mutual coupling regime, the circulator/LNA combination becomes increasingly effective at protecting the HPA. Analysis based on the measurements in Figure 12 shows that having an output power above 25 Watts ensures that the effective reflection coefficient off the LNA will always be less than the isolation specification of the circulator that will be used in the final system (25 dB), meaning that the LNA will act as an effective load in this power regime.



**Figure 13.** Rough determination of reflection coefficient off of RF frontend using measured and simulated antenna patterns.

### 3.4 Results of Two Element RF Panel

A panel subelement (2 by 1 radiators) was designed in its entirety. At its highest power, a single element of this system has shown radiation of 50 watts at 10% duty cycle, by turning the bias to 40 Volts. This was done with no heat sink other than a small copper block attached to the die without destructive testing. This, along with a small fan keeping the air moving past the amplifier, was sufficient to keep the temperature of the GaN package below 75°C. This demonstrates the potential for a low cost viable radar system.



**Figure 14.** 4 by 4 RF panel layout

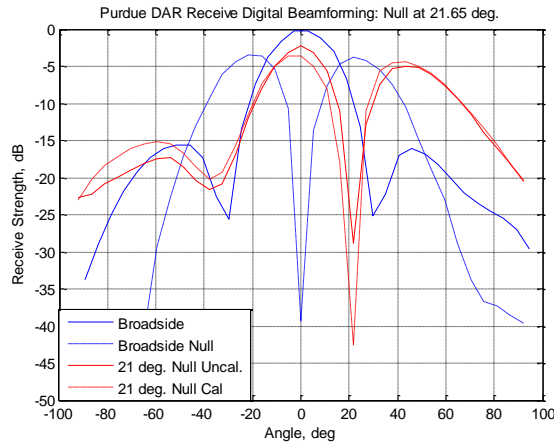
Although at present only the high power RF portion of the radar has been integrated on the panel, it is certainly feasible to consider including IF processing as well, due to the small size of the SiGe modulator/demodulator used for this project. This opens up possibilities for modular radar systems, in which an analog panel could be swapped out for one designed to operate in a totally different band but still using the same digital back-end.

## 4. IMPLEMENTATION OF A DIGITAL BEAMFORMER

In order to realize an effective digital beamformer, the digital backend, analog buffers, and transceiver must be aligned and calibrated. Calibration ensures proper I/Q gain/phase balance and DC offset on both transmit and receive, and the alignment process ensures that the correct amplitude and phase goes through each element, even in the presence of finite array and mutual coupling effect. On receive, the calibration and alignment can be performed automatically in the digital domain by applying a linear transformation to the received data stream on each element. On both transmit and receive in a finite array, the finite ground plane and mutual coupling effects lead to different element patterns for each element, which complicates the alignment process. However, there are many methods for mitigating these effects (see, for example, Kuehnke, 2001 and Kelley, 1993). The essence of these techniques is to use prior information and measurements about the array and system itself to determine the appropriate phases and weights for each element. This is completely trivial to implement in a digital system. In fact, pre-determined weights for a given pattern scanned in a given direction can be stored and applied very quickly in the digital backend.



An example of this is shown below in Figure 15. Calibration that accounted for the finite nature of the panel demo allowed for deep nulls in the response. Here, a partial version of the DAR system with a 4x1 receive array has been used to generate different patterns, including a broadside sum and a broadside null, shown in blue. A linear phase shift was then applied to scan the latter null pattern to 21.65 degrees, and the results are shown in solid red.



**Figure 15.** Received beam patterns from 4x1 array showing effects of different array alignment techniques

Notice that the null goes up more than 10 dB because of finite array/mutual coupling effects; this represents a 10dB hit in jammer suppression capability at this angle or a degradation in resolution if the radar is being used as a monopulse comparator. However, if the array is recalibrated to specifically have a good null at this scan angle, the null can be greatly improved without significantly altering the overall pattern, as shown in the dotted line. Once the correct weights for a given pattern are known, they can be stored for later use. Both transmit and receive calibration has been shown, indicating that the digital array is ready for further real-life testing.

## CONCLUSIONS

The use of a highly efficient GaN power amplifier coupled with a package that has a good thermal path enables the use of simpler cooling methods. This could involve a typical PCB fan at most duty cycles or even no active cooling at lower duty cycles. The GaN HPA is also able to operate at high temperatures without a significant loss in device performance. This has also been shown through testing a single element on an integrated radiating panel. The flexibility of the digital backend allows for the issues related to panel-level integration to be resolved through suitable calibration techniques. These initial tests are encouraging to the development toward the entire digital array radar system.

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